USER MANUAL

PXIe-8521

4-port, 100BASE-T1 PXI Automotive Ethernet Interface Module

This document explains how to install and configure the PXIe-8521 module.

Contents

Introduction

Kit Contents

- PXIe-8521 module
- 26 AWG x 8 mm insulated ferrules, x 20
- Screw driver for use with connector spring terminal push buttons
- *PXIe-8521 Safety, Environmental, and Regulatory Information*

Note The PXIe-8521 ships with plug connectors pre-installed on each port.

NATIONAL INSTRUMENTS

Getting Started

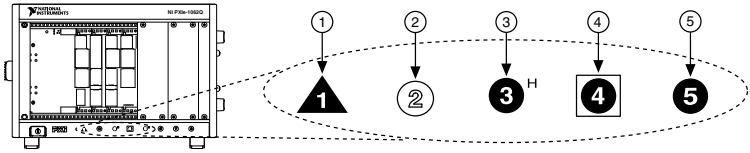
Installing the PXIe-8521

Notice To prevent damage to the PXIe-8521 caused by ESD or contamination, handle the module using the edges or the metal bracket.

1. Ensure the AC power source is connected to the chassis before installing the module.

   The AC power cord grounds the chassis and protects it from electrical damage while you install the module.
2. Power off the chassis.
3. Inspect the slot pins on the chassis backplane for any bends or damage prior to installation. Do not install a module if the backplane is damaged.
4. Remove the black plastic covers from all the captive screws on the module front panel.
5. Identify a supported slot in the chassis. The following figure shows the symbols that indicate the slot types.

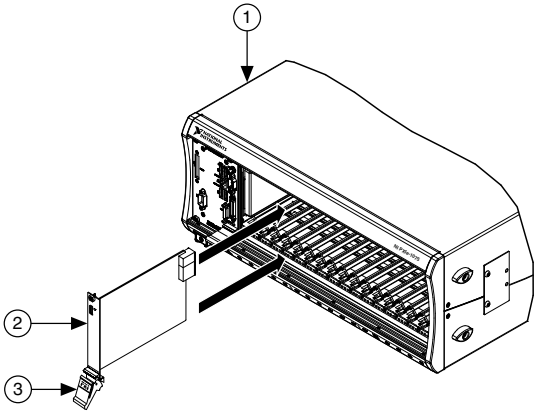
Figure 1. Chassis Compatibility Symbols



1. PXI Express System Controller Slot
2. PXI Peripheral Slot
3. PXI Express Hybrid Peripheral Slot
4. PXI Express System Timing Slot
5. PXI Express Peripheral Slot

   PXIe-8521 modules can be placed in PXI Express peripheral slots, PXI Express hybrid peripheral slots, or PXI Express system timing slots.
6. Touch any metal part of the chassis to discharge static electricity.
7. Ensure that the ejector handle is in the downward (unlatched) position.
8. Place the module edges into the module guides at the top and bottom of the chassis. Slide the module into the slot until it is fully inserted.

Figure 2. Module Installation



1. Chassis
2. Hardware Module
3. Ejector Handle in Downward (Unlatched) Position

9. Latch the module in place by pulling up on the ejector handle.
10. Secure the module front panel to the chassis using the front-panel mounting screws.

Note Tightening the top and bottom mounting screws increases mechanical stability and also electrically connects the front panel to the chassis, which can improve the signal quality and electromagnetic performance.

11. Cover all empty slots using EMC filler panels or fill using slot blockers to maximize cooling air flow, depending on your application.
12. Power on the chassis.

PXIe-8521 Pinout

Figure 3. PXIe-8521 Pinout

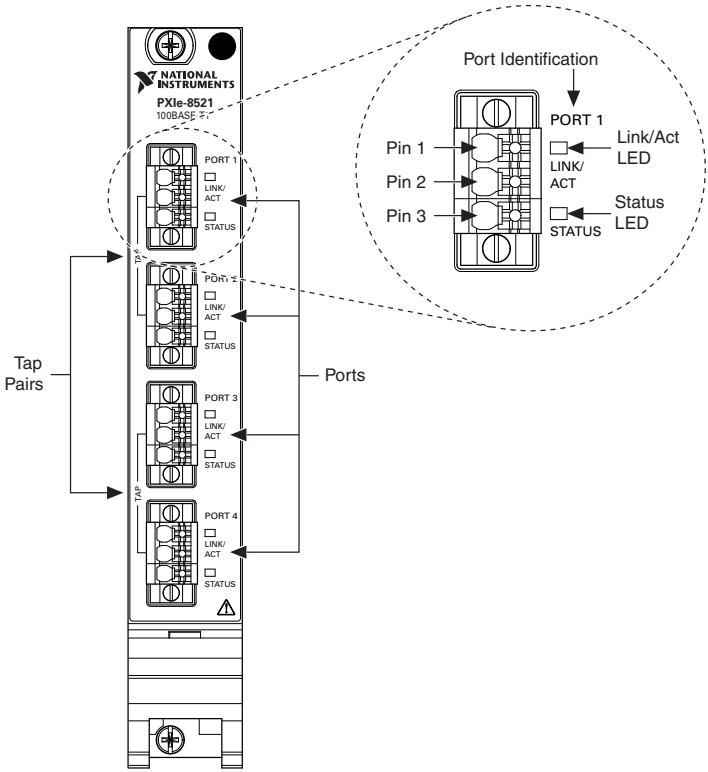


Table 1. PXIe-8521 Pinout Signal Descriptions

Pin Number	Signal Type	Signal Direction	Signal Description	Signal Required
1	TRX_P	Bi-directional	Transceiver plus	Required
2	TRX_M	Bi-directional	Transceiver minus	Required
3	Shield	—	Shield	Optional

Connection Guidelines

Notice Operate this product only with cables less than 15 m in length.

1. Push a solid wire or ferrule directly into the terminal.
2. When inserting a stranded wire without a ferrule, first open the terminal by pressing the push button with a finger or the included screwdriver tool.
3. Verify that all strands of a stranded wire are securely retained.
4. Insulated ferrules are recommended for small-gauge stranded wire. 26 AWG x 8 mm barrel length insulated ferrules are included with the product.

Note A ferrule crimping tool is not included with this product.

5. Tighten the connector screw flanges to the torque specification in the *PXIe-8521 Specifications* for the best shock and vibration performance. The connector screw flanges ship in a non-torqued configuration for easy removal.
6. When removing a wire, first open the terminal by pressing the push button with a finger or the included screwdriver tool.

Port Modes

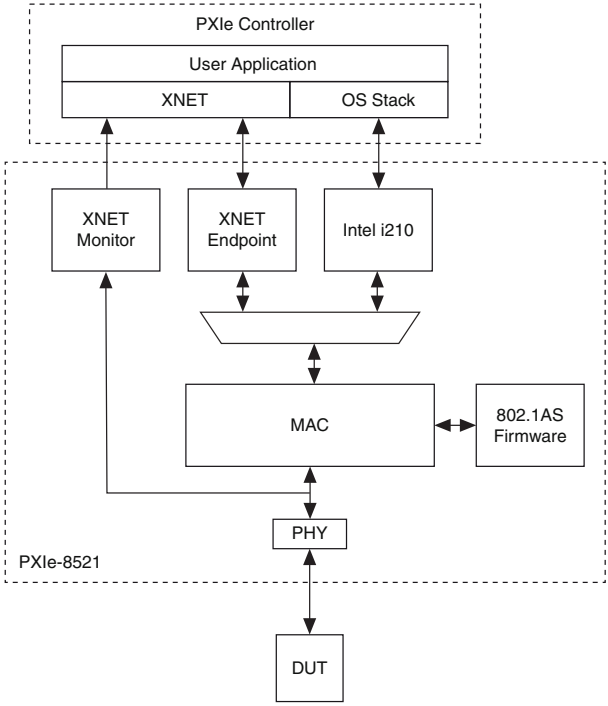
The PXIe-8521 includes four ports that can be configured as independent network interfaces on the module. The ports can function in Direct mode or Tap mode. Regardless of mode, traffic on each port can be monitored. When monitoring is enabled, all traffic that is transmitted or received on that port is captured. Each packet is timestamped by both the local time keeper and the port's network time keeper. The local time keeper runs off *PXI Clk10* if present on the chassis. Each port has an independent network time keeper, which uses IEEE 802.1AS to synchronize time with other devices on the network.

Note Port mode cannot be changed while an XNET session is started on the port. When the port mode is changed, port connectivity is lost while the change is configured.

Data Path Overview

The following diagram describes each port within the PXIe-8521.

Figure 4. PXIe-8521 Block Diagram



Each port has three data paths: XNET monitor, XNET endpoint, and OS stack. All three data paths can be used simultaneously depending on port mode. The monitor path reads and inspects all Ethernet frames that are received or transmitted on the port. The endpoint path transmits and receives Ethernet frames on the port. The endpoint path is typically used if you need it to act as an AVB endpoint. The OS stack path transmits and receives data using standard network sockets via the operating system's network stack. The OS stack is typically used with applications designed to use traditional TCP- or UDP-based protocols for its network communication.

Note The PXIe-8521 does not support jumbo frames.

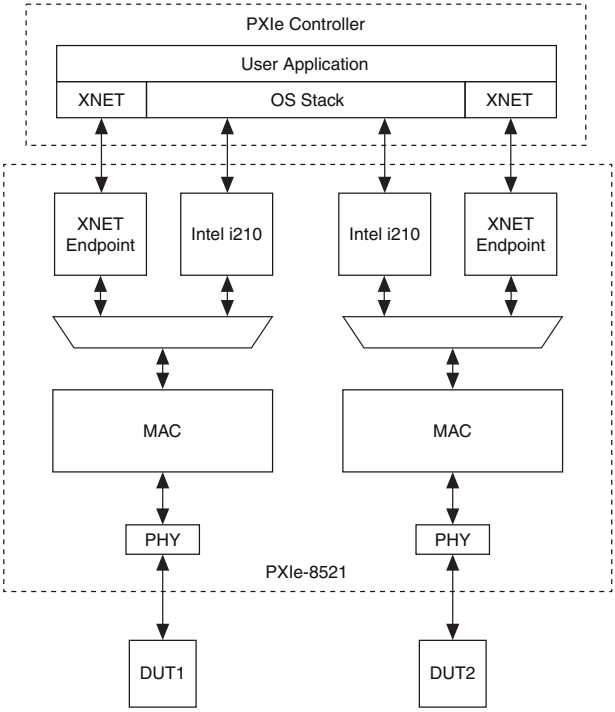
For Ethernet interfaces, the suffix "/monitor" indicates the use of a monitor path when it is appended to the interface name. For example, "ENET1" specifies use of the endpoint path, and "ENET1/ monitor" specifies use of the monitor path. The monitor path is used to read Ethernet frames that are received or transmitted on each port. When Tap is enabled, data received via the monitor path by a Tap pair will be identical on each port in the pair.

The IEEE 802.1AS protocol is implemented by the firmware running on the PXIe-8521, and packet timestamps are taken near the device's physical layer. This helps guarantee a high degree of synchronization accuracy for each port's network time.

Direct Mode

The following diagram describes Direct mode on the PXIe-8521.

Figure 5. Direct Mode



Note This diagram shows a design with two ports. Each of the device's four ports can run independently under Direct mode.

Note Although it is not shown in the diagram, you can simultaneously use the XNET monitor data path on each port while it is in Direct mode. This allows you to analyze all network traffic that is transmitted and received on the port's endpoint.

In *Direct mode*, ports are directly connected and function as endpoints; Ethernet frames received and transmitted on the port have no relationship to any other ports on the device. Input and output sessions are supported in Direct mode. The PXIe-8521 supports up to four ports using Direct mode.

Tap Mode

In *Tap mode*, a pair of adjacent ports on the device, called tap partners, are connected to form a Tap that allows the PXIe-8521 to monitor traffic. In Tap mode, physical Port 1 and Port 2 are

Tap partners, and Port 3 and Port 4 are Tap partners. A frame received on one Tap partner is transmitted out of the other Tap partner, which mimics the behavior of an Ethernet cable.

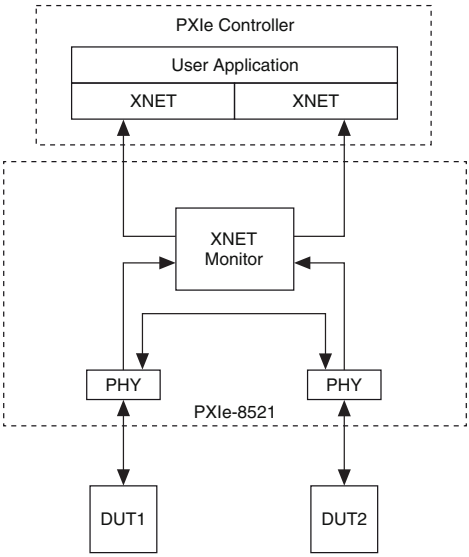
Note For more information about Tap latency, refer to the *PXIe-8521 Specifications*.

When an input session is created using an XNET interface for either Tap partner, and the "/monitor" suffix is used with the XNET interface, the session reads frames going through the Tap partners. Output sessions are not supported in Tap mode.

Note You only need to select the monitor of one port in the Tap pairing. If both monitors are selected, you will receive the same data twice.

Setting one port to Tap mode will automatically set the port's Tap partner to Tap mode. The PXIe-8521 supports two Taps (Ports 1/2 and Ports 3/4) using this mode. All four ports can also be used simultaneously while one pair is in Tap mode and the other ports are in Direct mode. The following diagram describes one Tap pair on the PXIe-8521.

Figure 6. Tap Mode



PHY State

The PXIe-8521 PHY's master/slave state can be configured for communication with its peer PHY. In traditional Ethernet networks, this master/slave state is negotiated automatically at the PHY level. However, in Automotive Ethernet networks such as IEEE 100BASE-T1, the master/slave state is commonly configured statically and is typically determined by the PHY state setting of the connected DUT. Configure the PHY state of the PXIe-8521's port to the opposite of the connected DUT's PHY state.

Configuring the PXIe-8521 in MAX

Use Measurement & Automation Explorer (MAX) to configure your National Instruments hardware. MAX informs other programs about which devices reside in the system and how they are configured.

1. Launch MAX.
2. In the configuration tree, expand **Devices and Interfaces** to see the list of installed NI hardware.

   Note If you do not see your module listed, press <F5> to refresh the list of installed modules. If the module is still not listed, power off the system, ensure the module is correctly installed, and restart.
3. Expand your module to see the list of ports.
4. Record the NI-XNET interface name that MAX assigns to each port of the hardware. Use this name when programming the PXIe-8521.
5. For each port, configure the port mode to either Direct or Tap, depending on whether you want to fully participate in network communication as an endpoint (Direct) or monitor an existing network connection (Tap).
6. For each port, configure the PHY state to either Master or Slave, depending on the corresponding state of the PHY that you are connecting to.

   Note Two PHYs that are physically connected must be configured to use opposing PHY states. One PHY must be configured to be the master, and the other PHY must be configured to be the slave.
7. Self-test the hardware by selecting the item in the configuration tree and clicking **Self-Test** in the MAX toolbar.

The MAX self-test performs a basic verification of hardware resources.

Programming the PXIe-8521

You can program the PXIe-8521 using both the NI-XNET API and the operating system's standard network stack API. Both APIs can be used simultaneously. Select an API based on the needed function, listed below:

API	Functionality
NI-XNET	• Monitor • AVB endpoint • IEEE 802.1AS synchronization • Trigger synchronization • Port configuration
Operating System Network Stack	• Network sockets (TCP/IP and UDP/IP)

NI-XNET provides many of the advanced data access and timing & synchronization capabilities for the device, while availability of the OS network stack provides a

straightforward way to integrate applications that rely on standard network sockets for their network communication.

LED Functionality

The PXIe-8521 includes two LED indicators per port to help you monitor hardware and bus status.

LED Label	LED State	LED Color	Condition
LINK/ACT	Off	—	No link established Default power-up state
	Solid	Green	Link established, 100 Mbits/s
	Blinking	Green	Activity, 100 Mbits/s
STATUS	Off	—	Default power-up state
	Solid	Green	Direct Mode, master (PHY state)
		Amber	Direct Mode, slave (PHY state)
	Fade in and out[1]	Green	Tap Mode, master (PHY state)
		Amber	Tap Mode, slave (PHY state)
	Blinking	Green	Port ID
		Amber	Not synchronized
		Red	Catastrophic error[2]

Synchronization Methods

The PXI and PXI Express chassis feature a dedicated synchronization bus integrated into the backplane. NI-XNET products support use of this bus to synchronize with other National Instruments hardware products such as DAQ, IMAQ, and NI Motion Control. The PXI synchronization bus consists of a flexible interconnect scheme for sharing timing and triggering signals in a system.

Local Time

The PXIe-8521 uses PXI_Clk10, a 10 MHz PXI backplane clock, to drive the local time keeper and to synchronize with other modules in the PXI chassis. If the PXI backplane clock is not available, the PXIe-8521 uses an internal oscillator.

[1] When in Tap Mode, ports that are paired fade in phase with each other, but out of phase with other ports.

[2] In the case of a catastrophic error, recover by invoking Reset on the module in MAX. Contact NI for further support if the error continues to occur.

PXI_Clk10 provides frequency but not date/time information. When an NI-XNET session is created, XNET initializes the date/time information for the local clock using host time.

Network Time

In addition to the local time keeper, the PXIe-8521 can maintain network time (IEEE 802.1AS) for each port. When Ethernet frames are received, each packet is timestamped with network time as well as with local time.

When a port acts as a master in an electronic control unit (ECU) network, the network time is initialized from host time and is synchronized to local time.

When a port acts as a slave in an ECU network, local time and network time may eventually drift relative to each other. The date/time information for network time is obtained from the ECU that acts as the grandmaster clock.

Both local and network time can be adjusted using the NI-XNET API.

Host Time

Host time is the clock of the operating system on which the NI-XNET driver is running. The host time can obtain time/date information using a real time clock (RTC) or a network time protocol (NTP) server.

Although host time provides accurate date/time information, the accuracy and resolution of its clock can often be in tens of milliseconds. In contrast, the PXIe-8521 provides resolution for local time and network time in nanoseconds. Although local time and network time use host time to initialize their date/time information, they do not use the same physical clock as host time. Therefore, both local time and network time may eventually drift relative to host time.

PXI Triggers

Each of the eight PXI triggers on the PXIe-8521 can be simultaneously timestamped by the local time keeper and the network time keeper for each port. PXI triggers can be used to synchronize the PXIe-8521 time keepers with trigger events on other PXI modules.

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